A PSEUDO-CLASS-AB TELESCOPIC-CASCODE OPERATIONAL AMPLIFIER

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ABSTRACT

A novel class-AB architecture for single-stage operational amplifiers is presented. The structure employs a switched-capacitor level shifter to provide a signal-dependent current in the current source of the common-source amplifier. Applying this pseudo-class-AB approach to a telescopic-cascode op-amp enhances the effective values of the slew rate and the transconductance and thus the op-amp speed.

1. INTRODUCTION

An operational amplifier, the most commonly used and often the most power-hungry building block in a mixed-signal system, can be a suitable candidate to apply low-power design techniques. Telescopic cascode op-amp typically has a better bandwidth/power-consumption performance than other topologies [1]. In a telescopic cascode op-amp, the output slew rate is determined by I_{tail} / C_L where I_{tail} and C_L are the tail current and the load capacitance of the op-amp, respectively. Therefore, the current value should be increased in order to enhance the slew-rate of the op-amp for a particular value of the load capacitance. Hence, circuit techniques enhancing the op-amp slew-rate would be useful in reducing its power consumption.

In this paper, a novel fully-differential class-AB telescopic-cascode op-amp is proposed, which considerably reduces the power consumption in high-speed op-amps driving large capacitive load. Using the proposed class-AB technique, the current value of the load current source will be dynamically increased when needed. Therefore, the effective values of the trans-conductance and the slew rate are increased and the performance speed of the op-amp is increased. For a constant operating speed, the quiescent current value of the single-stage op-amp or that of the second stage of a two-stage op-amp can be chosen smaller employing the proposed class-AB stage.

2. CLASS-AB OUTPUT STAGE

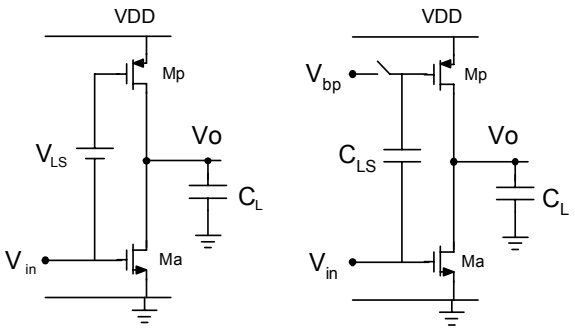
There have been several methods usually in two-stage op-amps, to improve the slewing behavior of the circuit. One of them is the class-AB structure. The basis of the idea is to apply the signal to both sink and source output transistors of the common-source output stage of two-stage op-amp, i.e. to provide a signal-dependent current for the current source in the common-source amplifier.

In one popular implementation of class-A/AB amplifiers [2, 3], additional current mirror circuits are employed to apply the signal to both output transistors. There are some disadvantages along with these class-A/AB stages. A relatively small mirror pole in the signal path is added to the system due to the current mirror circuit, which may degrade the frequency behavior of the op-amp. The current of this current mirror stage cannot be chosen much smaller than the output stage not to make the mirror pole too small to degrade the frequency response. Thus some power is added as well. This op-amp also needs an additional common-mode feedback leading to additional power and area.

3. THE PROPOSED APPROACH

A novel yet very simple class-AB stage is proposed here that omits the additional stage of the conventional structures and can be applied to single-stage op-amps as well. Such a configuration can be easily employed in operational amplifiers used in switched-capacitor circuits where the op-amp is usually idle in half a cycle. The general schematic and a possible implementation of the circuit are shown in Figure 1. It is obvious that if a suitable bias voltage is added to the input signal to be appropriate for applying to the pMOS transistor of Figure 1-a, the circuit works as a class AB amplifier. In one implementation of the approach, depicted in Figure 1-b, a level-shifting capacitor, C_{LS} is utilized which is charged with the bias voltage of the pMOS current source minus the bias gate-to-source voltage of the nMOS amplifying device in the sampling phase when the op-amp is idle. In the amplifying phase, the switch is disconnected and assuming little charge leakage for the capacitor, the pMOS current source is biased with a suitable voltage that is signal-dependent as well. When the signal goes down, since C_{LS} acts as a level shifter, the gate voltage of the pMOS current source also goes down so it will source more current in order to quickly charge the output capacitance. To ensure that the voltage across the level-shifting capacitor remains unchanged, the capacitor value is chosen enough larger than the parasitic capacitance at the gate node of the pMOS device of Figure 1. In the proposed structure the equivalent transconductance of the stage, g_{mT} is obtained from

$$g_{mT} = g_{m_{Ma}} + g_{m_{Mp}} \tag{1}$$



(a) (b)

Figure 1. (a) The general schematic, (b) a possible implementation of the proposed switched-capacitor class-AB stage

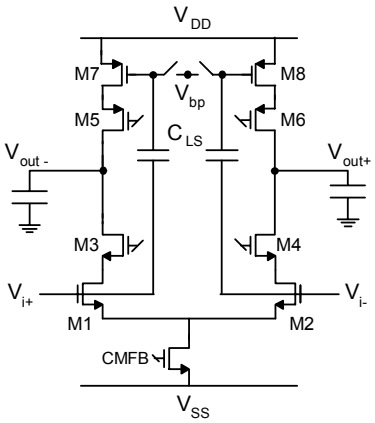


Figure 2. The proposed telescopic-cascode class-AB op-amp schematic

Such an approach can be applied to the single-stage op-amps, for example telescopic cascode op-amp as depicted in Figure 2. If a large signal is applied to the inputs of the op-amp, one of the input transistors (for example *M*1) will turn ON and *M*2 turns OFF. In addition, due to the proposed structure applied to the op-amp, the transistors *M*7 turns OFF and *M*8 turns ON. Writing KCL at the V_{out+} node, it can be easily shown that C_L is discharged by I_{tail} instead of $I_{tail}/2$ (the case in the traditional telescopic-cascode configuration). Therefore, the slew rate of the new pseudo-class-AB telescopic cascode op-amp is generally doubled compared to the traditional telescopic architecture. Note that the current enhancement is limited to 2, thus the expression *pseudo*-class-AB is employed. As mentioned before in (1), the structure will improve the equivalent value of the stage transconductance, g_{mT} leading to more gain and bandwidth for the op-amp. This is another important advantage of this structure.

The main drawback of the structure presented here is the comparatively large capacitor, C_{LS}, utilized for level shifting. However, it should be regarded that the new approach has already saved some area occupied by the mirror branch utilized in the traditional class-AB stages. The other drawback of such architecture is the degraded power-supply rejection ratio (PSRR). The power-supply noise can be directly amplified through *M*7 and *M*8 to the outputs. However, using symmetric layout considerations in this fully-differential structure, the power-supply rejection ratio can be improved.

4. SIMULATION RESULTS

In order to verify the behavior of the proposed op-amp, it is employed in a 3.3-V flip-around sample and hold circuit of a 12-bit 100 MS/s pipeline analog-to-digital converter. In the designed op-amp, the load capacitance including the input capacitance of the first residue amplifier of the ADC, the equivalent capacitances due to the feedback capacitor and the output parasitic capacitance of the op-amp is about 8pF. In addition, C_{LS} is chosen equal to 3pF to satisfy the level shifting behavior. The switches employed for level shifting are simple small-size pMOS transistors to avoid switch charge injection. It is obvious that in the

holding mode, the capacitor C_{LS} is connected in series with the gate capacitance of $M7$ or $M8$ and so the input capacitance of the op-amp is approximately doubled.

This sample-and-hold amplifier is simulated with HSpice in all process corners using BSIM3v3 models of a 0.35-µm CMOS process. Figure 3 shows the frequency response of the op-amp employed in the SHA. To model the frequency behavior of the op-amp, the switches of the switched-capacitor level shifter are replaced with large resistors. According to Figure 3, the gain and phase margin of the op-amp are 76dB and 67.5˚, respectively. The full-swing step response of the circuit is depicted in Figure 4-I. It shows that the worst-case 0.024% settling time of a full-swing signal is less than 4.5 ns. Figure 4-II shows the current waveform of the transistors $M7$ and $M8$ while settling, illustrating the class AB behavior of the op-amp. The total worst-case power consumption of the sample and hold amplifier is less than 16mW. The output spectrum of the SHA with a Nyquist input is depicted in Figure 5. It shows that the worst case SNDR and SFDR are better than 85 dB and 91 dB, respectively. Table 1 summarizes the proposed SHA specifications. Comparing the achieved specifications with a few recent reports [4-6], it can be observed that the presented class-AB technique has been effective to reduce the power consumption of the SHA with comparable speed, accuracy, and V_{DD} parameters.

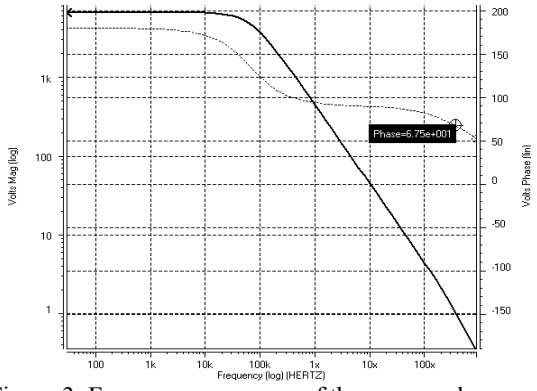


Figure 3. Frequency response of the proposed op-amp

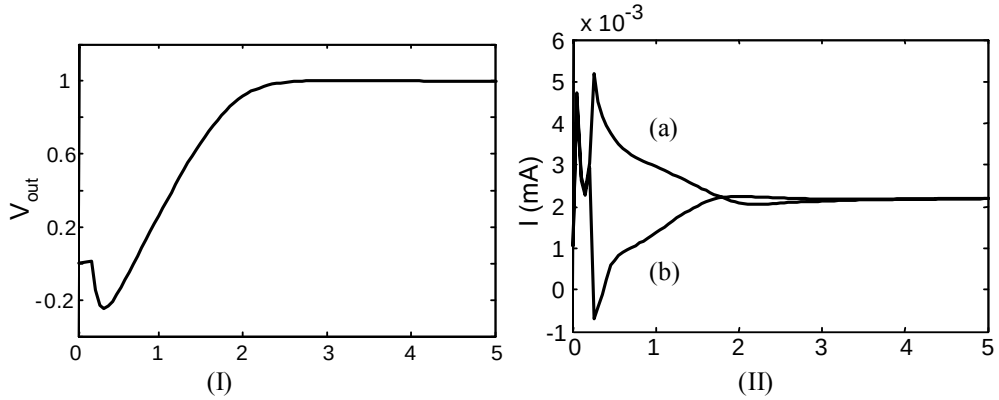


Figure 4. (I) Simulated step response of the SHA, (II) Current consumption while settling, (a)&(b) in $M8$ and $M7$ pMOS transistors.

Table 1. Proposed SHA specifications

Op-amp gain	76dB
Op-amp Phase Margin (β=1)	67.5°
Total load capacitance	8pF
Total power consumption	16 mW (@V_{DD}=3.3V)
Level shifter capacitor	3pF
Settling time (0.024%)	4.5ns
SHA SFDR	91 dB
SHA SNDR	85 dB

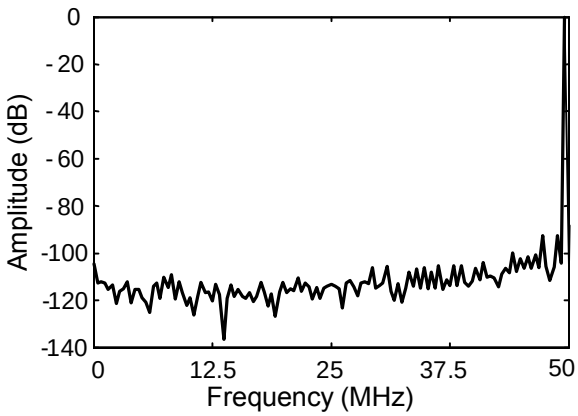


Figure 5. Simulated output spectrum with a Nyquist-frequency full-swing input

5. CONCLUSIONS

In this paper, a new configuration for a class-AB stage is presented and a novel low-power fast-settling op-amp is designed. Using a level-shifting switched capacitor, signal-dependent bias voltage is provided for the current source in a common-source or cascode amplifier. HSpice simulation results of a 100MS/s SHA employing the proposed telescopic-cascode op-amp, confirm the effectiveness of the proposed pseudo-class-AB architecture in power reduction of the operational amplifiers.

6. REFERENCES

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