A Flexible Model of a CMOS Field Programmable Transistor Array Targeted for Hardware Evolution

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Abstract. *This article focuses on the properties of a fine grained re-configurable transistor array currently under test at the Jet Propulsion Laboratory (JPL). This Field Programmable Transistor Array (FPTA), is integrated on a Complementary Metal-Oxide Semiconductor (CMOS) chip. The FPTA displays advantageous features for hardware evolutionary experiments when comparing to programmable circuits with a coarse level of granularity. Even though this programmable chip is configured at a transistor level, its architecture is flexible enough to implement standard analog and digital circuits' building blocks with a higher level of complexity. This model and a first set of evolutionary experiments have been recently introduced; here, the objective is further illustrating its flexibility and versatility for the implementation of a variety of circuits in comparison with other models of re-configurable circuits. Some evolutionary experiments are also presented, serving as a basis for the authors to devise an improved model for the FPTA, to be manufactured in a near future.*

1 Introduction

In the context of Evolvable Hardware, researchers have been using programmable circuits as platforms for their experiments. These programmable circuits are divided into two classes, Field Programmable Gate Arrays (FPGAs) and Field Programmable Analog Arrays (FPAAs). The former is intended to be used in the digital domain, and the latter in the analog domain. Both the *FPGAs* and the *FPAAs* commercially available have a coarse granularity, which may restrict the potential of evolutionary design to the achievement of well-known topologies possible with such components. In order to overcome this problem, a fine-grained model of programmable circuit is being tested at JPL. This programmable device, called FPTA, gets the benefits of reconfiguration at the transistor

level, the use of CMOS technology, and the possibility of synthesizing circuits in the analog and in the digital domain. A first version of this programmable chip has already been successfully employed in the evolution of a computational circuit [11].

The purpose of this paper is twofold: to highlight the advantages of a fine-grained architecture for programmable circuits, which is also able to provide circuits with higher levels of granularity as building blocks for evolution; and presenting some preliminary evolutionary experiments in the synthesis of certain circuits whose main characteristics are analyzed in different domains. The capacity of mapping circuits of higher complexity, whilst being programmable at the transistor level, gives the designer the possibility to choose the most adequate building blocks to be manipulated by the evolutionary algorithm. Additionally, the evolution of circuits in different analysis' domains shows the flexibility of this model to accomplish the synthesis of a wide variety of electronic circuits.

This paper is divided in the following way: the second section briefly summarizes some models of programmable circuits; section 3 reviews the basic features of the programmable device developed at JPL; section 4 describes the mapping of some standard circuit building blocks into this FPTA; section 5 presents two evolutionary experiments, where the FPTA is used as a model to synthesize circuits in different domains of analysis. An enhanced model of the FPTA is also introduced in this section. Section 6 concludes the work, and describes future developments and applications of this re-configurable platform.

2 Reconfigurable Circuits

Field Programmable Analog Arrays and *Field Programmable Gate Arrays* promise to establish a new trend in electronic design, where a single device has now the flexibility to implement a wide range of electronic circuits. While FPGAs have been developed for applications in the domain of digital signal processing and re-configurable computing, most FPAA models are being developed for applications in programmable mixed-signal circuits and filtering. In addition to the intrinsic flexibility of these devices, which confers advantageous features to standard electronic design, FPGAs and FPAAs are also the focus of research in the area of *self programmable* systems [3][7][12]. Particularly, genetic algorithms are the main agent employed to promote the property of automatic configuration.

Nevertheless, there are many issues that should be addressed prior to using a programmable circuit in the context of artificial evolution. Perhaps, the most important of these issues is the one of the granularity of the programmable chip. The devices presented so far can be divided into two classes, coarse grained and fine grain devices. While the former uses more complex circuits, such as digital gates and operational amplifiers, as the building blocks for the design process, the latter is configurable at a lower level, usually the one of transistors.

Most FPGA models consist of an arrangement of cells that perform digital logic, such as basic gates, multiplexers and flip-flops [7]. The user can configure the cells'

connections and, in some models, their functionality. Many surveys of FPGA models can be found in the literature [12]; therefore, this section focuses on the description of FPAAs, whose development has occurred more recently. Five models are now described.

2.1 TRAC – Totally Re-configurable Analogue Hardware

This device, manufactured by Zetex, is a coarse grained FPAA, consisting of twenty operational amplifiers laid out as two parallel sets of ten inter-connectable amplifiers [2]. Each amplifier has various components around it that may be switched in and out of circuit, by programming a shift-register to give one of eight distinct operations: off; pass; invert; exponentiation; logarithm; rectify; and sum of two inputs. The Zetex programmable chip has been used in evolutionary experiments that targeted the synthesis of a particular input-output voltage characteristic [2], rectifiers, and others [8].

2.2 Motorola Field Programmable Analog Array (MPAA020)

Another example of a coarse grained FPAA is the MPAA020 chip introduced by Motorola[4]. The analog resources of this chip are distributed along 20 cells almost identical among one another. Each cell includes the following hardware resources: one CMOS operational amplifier; one comparator; capacitors; programmable switches; and SRAM. This is the hardware required to the design of switched capacitor based circuits. This FPAA is configured by a bitstring of 6864 bits that control the circuit connectivity, capacitors' values and other features. A single block can be used to implement amplifiers, adders, subtractors, rectifiers, sample and hold circuits and first-order filters. More complex functions, such as biquad filters, PLLs and level detectors, can be implemented using two or more cells from this chip. This programmable chip has been used as a platform for the evolution of filters, oscillators, amplifiers, and rectifiers [13].

2.3 Palmo (University of Edinburgh)

Another coarse-grained FPAA chip is the one devised by the research group of the University of Edinburgh, the *Palmo* development system [1]. This chip works on pulse-based techniques, which constitute a more distinctive approach to implement signal processing functions. Instead of representing signals as voltages or currents, digital pulses are used to represent discrete analog signals in this programmable analog array. The magnitude of the discrete analog signal is encoded in the width of the pulse. The sign of the signal is determined by whether the pulse occurs in the positive or negative cycle of a global sign clock. The *Palmo* chip is constituted by an array of programmable cells that perform the functionality of integrators. As reported in [1], recent *Palmo* devices have been implemented in BiCMOS technology, being operated at 5 Volts and at a sampling frequency of 5MHz. As the designers remark, the use of BiCMOS technology will possibly allow the system to be operated at sampling frequencies around 20MHz.

2.4 Evolvable Motherboard (University of Sussex)

The Evolvable Motherboard (EM) [5] is a research tool developed at the University of Sussex, intended to the implementation of artificial evolutionary experiments. Unlike the

previous models above described, the EM presents a lower level granularity. This programmable circuit allows a large variety of electronic components to be used as the basic circuit elements, such as bipolar transistors, resistors and capacitors. This re-configurable board is organized as a matrix of components, where digitally controlled analog switches allow row/column interconnection. Depending on the particular application, the number of switches can be enough to cover all possible combinations of interconnections. The EM design explores non-idealities of the analog switches, such as parasitic resistances and capacitances. As described in [12], connections made using the analog switches have resistance and capacitance, hence, forming an integral part of any circuit configured. In the total, approximately 1500 switches are used, giving a search space of 10^{420} possible circuits. The EM has already been used in evolutionary experiments whose objectives were the design of inverter gates[12], amplifiers and oscillators.

2.5 – Lattice Programmable Analog Circuits (PACs)

The Lattice PAC is a coarse-grained programmable analog circuit that was commercially introduced recently [6]. The basic active functional element of these devices is the PAC cell, which, depending on the specific device architecture, may be an instrumentation amplifier, summing amplifier or other elemental active stage. Analog function models, called PAC blocks, are constructed from multiple PAC cells to replace traditional analog components such as amplifiers and active filters, eliminating the need for most external resistors and capacitors. Requiring no external components, it can be used to implement basic analog functions, such as precision filtering, summing/differencing, gain/attenuation, and conversion. The Lattice PAC architecture is similar to the one of the MPAA020 from Motorola, with the exception that, in the latter, resistors are implemented through switching capacitors.

3 Field Programmable Transistor Array (FPTA)

The authors believe the FPGAs and FPAAs commercially available in the current moment are not the more adequate solution for Evolvable Hardware applications. Most of them are coarse grained devices, based either on operational amplifiers or digital gates. This constrains evolution to sample designs based on human conceived building blocks, even though they may sometimes behave in an unexpected way [12]. The transistor array described in this paper combines the features of a fine granularity, being programmable at the transistor level, with the architectural versatility for the implementation of standard building blocks for analog and digital design.

The Field Programmable Transistor Array is a fine-grained re-configurable architecture, being particularly targeted for Evolvable Hardware experiments. The basic components are MOS transistors, integrated in a chip using 0.5-micron CMOS technology [10]. As both analog and digital CMOS circuits ultimately rely on functions implemented with transistors, the FPTA appears as a versatile platform for the synthesis of both analog and digital (and mixed-signal) circuits. Moreover, as it will be

demonstrated in the next section, the FPTA architecture is also flexible enough to provide more complex building blocks to the evolutionary system.

The FPTA cell is an array of transistors interconnected by programmable switches. The status of the switches (ON or OFF) determines a circuit topology and, consequently, a specific response. Figure 1 illustrates an example of a FPTA cell consisting of 8 transistors and 24 programmable switches. This cell consists of PMOS and NMOS transistors, and switch based connections. As it will be further described in this paper, this cell architecture allows the synthesis of both standard and novel topologies for some basic circuits. According to the outcome of the experiments being currently performed, a slightly different architecture may be proposed for the next version of the FPTA.

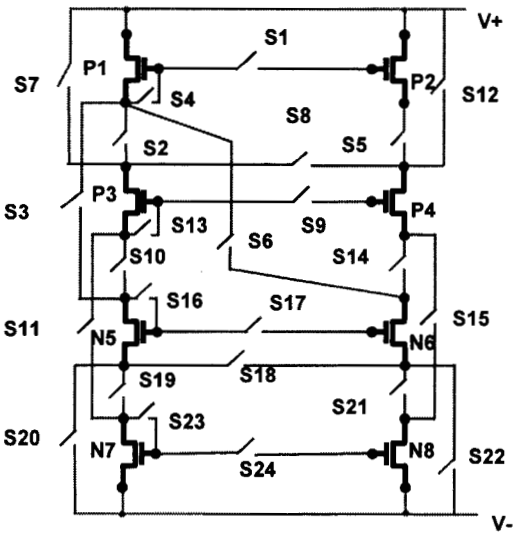

Fig. 1 – Schematic of a FPTA cell consisting of 8 transistors and 24 switches.

The programmable switches are implemented with transistors acting as transmission gates. The switches can either be programmed for the implementation of minimal and maximal resistance values, by applying 0V and 5V at the transistors' gates, or they can be programmed to implement intermediate resistance values, by applying values between 0V and 5V at the transistors' gates. Preliminary experiments suggest that the use of intermediate values for switching control generates a smoother fitness landscape [11].

4 Mapping Standard Circuit Building Blocks Into the FPTA

This section describes the mapping of some standard circuit building blocks into the FPTA. The objective is to show that the architecture depicted in Figure 1 is flexible

enough to implement basic structures used in analog and digital design. We depict here the implementation of three cells: a basic common-source amplifier; a transconductance amplifier; and an AND digital gate. Those are examples of circuits that can be optionally used as building blocks for the evolution of analog and digital circuits.

Figure 2.A depicts the FPTA configuration for a common source amplifier implementation. This circuit is employed to provide voltage gain. This structure can be easily mapped into one cell of the transistor array. As shown in the figure below, transistors P3 and P4 form a current mirror pair that works as the active load for the amplifying transistor, N6. The current level is determined by the input voltage *Vbias*, applied at the gate of the transistor N5, which serves as an active resistance for the current mirror. Figure 2.B compares the DC transfer function of these circuits in two cases: simulation and real implementation. In the former, we use PSPICE to simulate the amplifier without switches implementing the connections; in the latter, we get real data from the amplifier implementation. Therefore, we compare the implemented version with an ideal one.

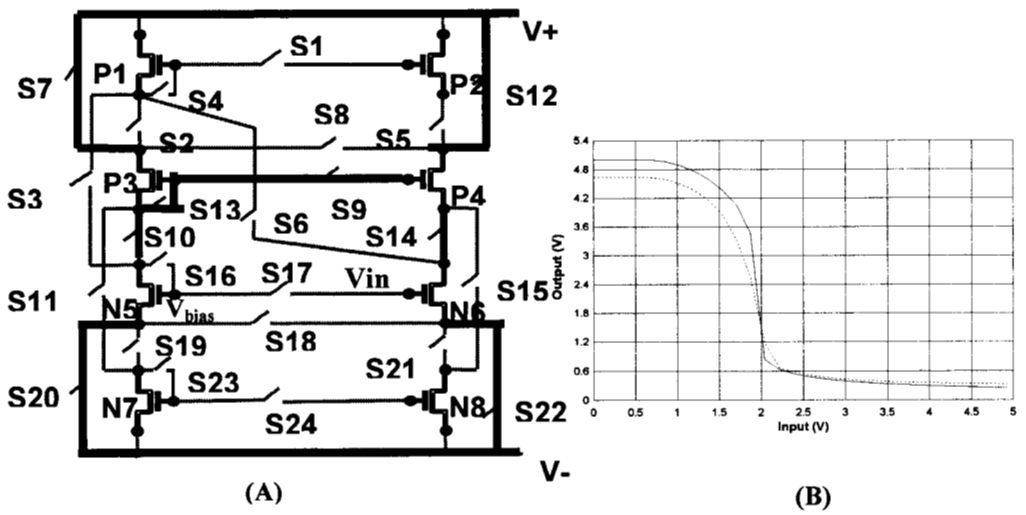

Fig. 2 – (A) - Schematic of the mapping of a basic common source amplifier into the FPTA. (B) - DC transfer of the common source in simulation (full line) and the one implemented in the FPTA (traces).

From Figure 2 we can observe that the transfer curves of the two circuits' versions have the shape of an inverter amplifier. They only differ in their higher saturation value, 5V for the simulated circuit and 4.6V for the real circuit. This difference is due to the fact that the circuit is very sensitive to the DC operating point, given by the current bias.

Another circuit building block that can be easily mapped into the FPTA is the transconductance amplifier, whose schematic is displayed in Figure 3. Also shown in

Figure 3 is the graph comparing the DC transfer functions between the tranconductance amplifier implemented in the FPTA and a simulated version of the same with no switches.

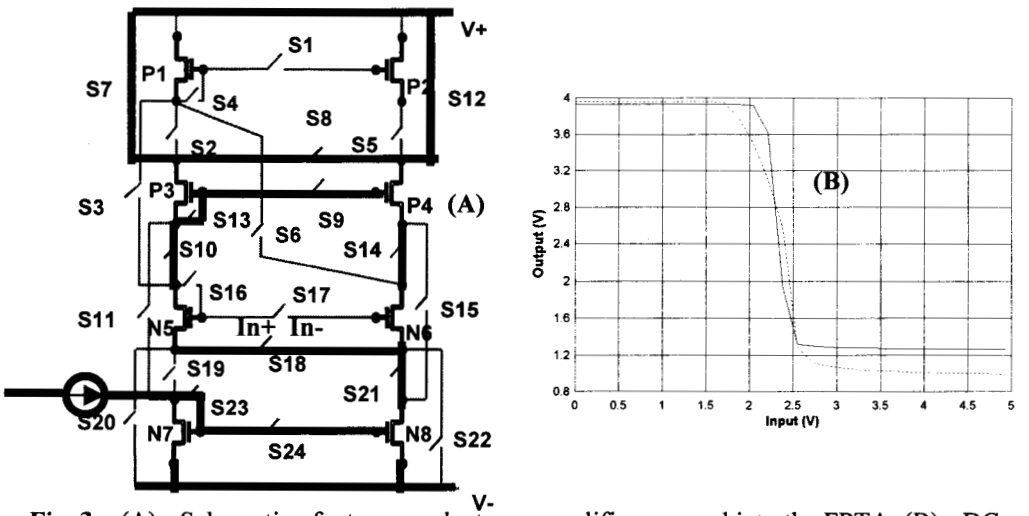

Fig. 3 – (A) - Schematic of a transconductance amplifier mapped into the FPTA; (B) - DC transfer of the circuit in simulation (full line) and the one implemented in the FPTA (traces).

Figure 4 displays the schematic of a digital gate mapped into two cells of the FPTA. This digital gate performs NAND/AND operations over the inputs *In1* and *In2*, as shown in the figure below. This circuit was implemented in the FPTA, working as expected.

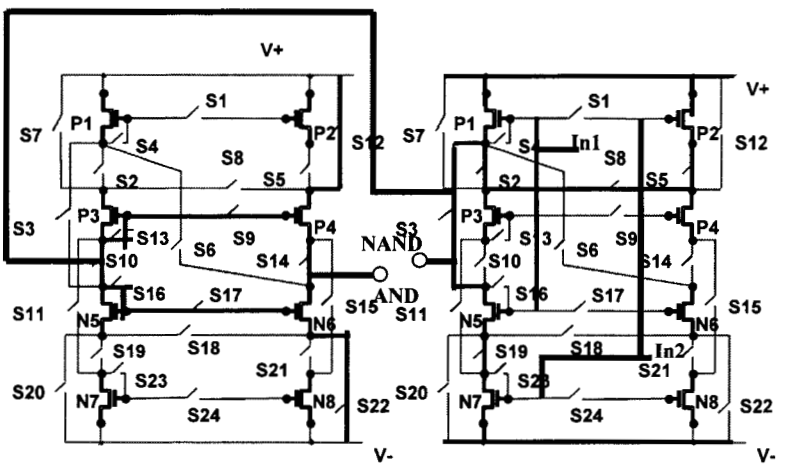

Fig. 4 – Schematic of an AND gate mapped into two FPTA cells.

5 Evolutionary Experiments

This section describes two evolutionary experiments carried on using the FPTA model in the *PSPICE* simulator: the evolution of an amplifier and of a band-pass filter respectively. In the former, the objective has been to synthesize a circuit with the DC transfer characteristic typical of an amplifier, similar to the ones illustrated in the last section. One way to accomplish this task is by using the following fitness evaluation function:

$$\text{Fitness} = \text{Max}_{i=1}^{n-1} |V(i+1) - V(i)| \qquad (1)$$

Where V(i) describes the circuit output voltage as a function of the DC analysis index i, which spans the swept range of the input signal, i.e., from 0 to 5 Volts. This evaluation function aims to identify the maximum voltage gradients between consecutive input voltage steps, the larger the gradient, the larger the amplifier gain will be [12]. This fitness evaluation function does not impose a DC operating point for the amplifier. Figure 5 depicts the schematic of the evolved circuit, together with the DC transfer responses achieved in the FPTA implementation and in simulation.

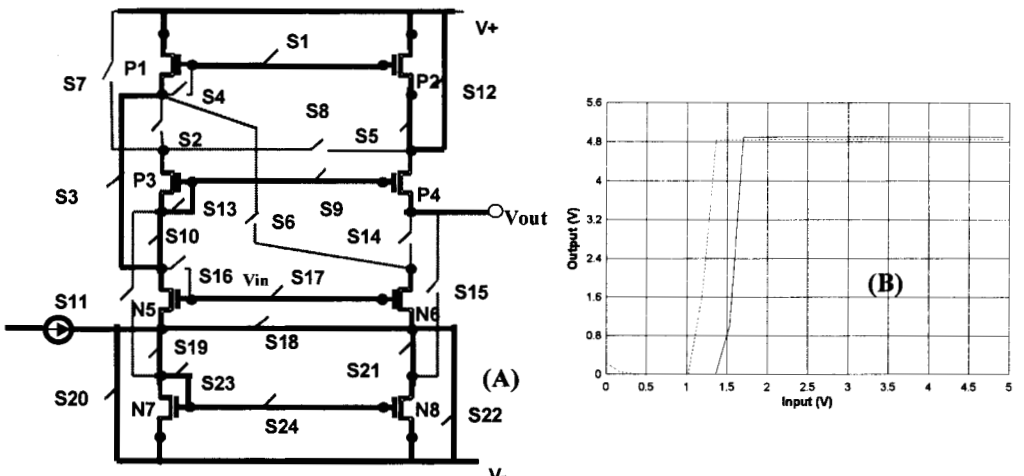

Fig. 5 – Schematic of an evolved amplifier using the FPTA model (A); comparison of the DC characteristic displayed by the simulated and implemented versions of the amplifier (B).

This result compares very well with the one reported in [12], where the same fitness function was used, but the basic elements for evolution were bipolar transistors and resistors. While, using the FPTA, only 900 evaluations (30 individuals along 30

generations) were necessary, around 10^4 evaluations were needed to obtain a similar DC transfer function in [12]. In addition, the evolved circuit shown above can be directly implemented in a CMOS re-configurable chip.

The second evolutionary experiment targeted the synthesis of a band-pass filter for the AM band, whose range goes from 150kHz to 1MHz. Since the basic FPTA model does not include large capacitances (only low-valued parasitic transistors' capacitances), we included external capacitances in the basic cell, based on a previously evolved filter [14]. In addition, instead of using values of 0V and 5V to control the switches, intermediate values of 1.5V and 3.5V were employed in this experiment. By doing so, intermediate active resistance values (100K and 10K) can be achieved, improving the performance of the FPTA for filter design. Figure 6 depicts the evolved filter and its frequency response. In the circuit schematic, we can see that the switches were replaced by resistances.

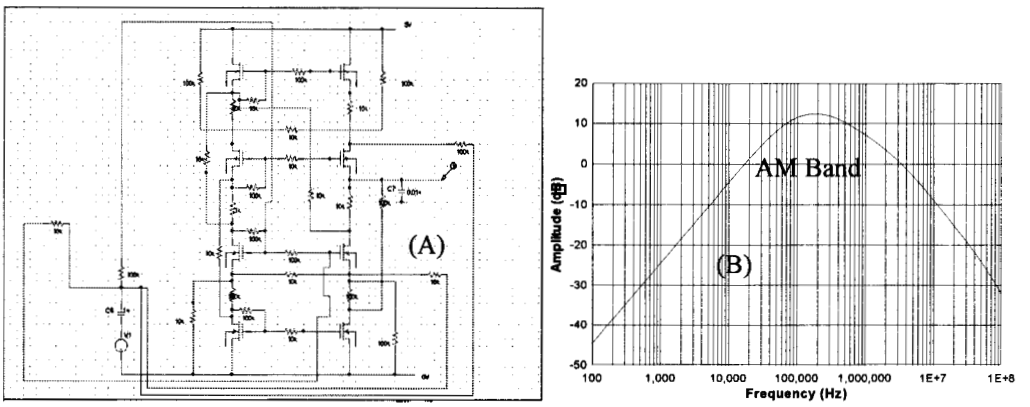

Fig. 6 – (A) - Schematic of an evolved band-pass using an enhanced FPTA model; (B) – Frequency response.

From the schematic of the above figure, it can be seen that this model differs from the previous one in the following aspects: an output capacitance and a de-coupling capacitance were added; and multiple paths from the input signal to the main circuit were allowed. We remark that the Genetic Algorithm did not depart from scratch in this application, because both capacitors' position and values were known a priori from another evolved design [14]. However, the final frequency response is well centered within the AM band, providing a gain of around 15 dB (typical of human made design for this circuit). This FPTA model is probably the basis of a forthcoming new project, which will include capacitors' arrays and all the resources needed for the evolution of a wide variety of analog and digital circuits.

6 Conclusions

This paper presented a programmable chip whose development is oriented towards the achievement of an adequate tool for hardware evolution. It was shown that the FPTA architecture is flexible enough to map basic analog and digital circuits building blocks, such as transconductance amplifiers and digital gates. In addition, this model gets the benefits of programmability at the transistor level. The authors feel encouraged to enhance the FPTA model in order to accomplish the evolution of complex systems.

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