Design of the QBIC wearable computing platform

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Abstract

Wearable computing systems can be broadly defined as mobile electronic devices that can be unobtrusively embedded in a user's outfit as part of the garment or an accessory. Unlike conventional mobile devices, such systems shall be virtually invisible, not hindering physical activity, always active and running without user's attention.

We present our wearability driven design approach and the philosophy for a novel wearable computing system integrated into a fully functional belt. This system integrates the main electronics in the buckle of a belt and utilizes the belt itself as extension bus and mechanical support for add ons. The system runs GNU/Linux operating system and has sufficient resources to address a variety of applications in the field of wearable computing. Considerations regarding ergonomic design, system architecture and first implementation results and applications are presented.

1 Introduction

1.1 Wearable computing systems

Despite rapid progress in miniaturization and increasing performance today's hand-held computers and other consumer electronic devices still have two major drawbacks: bulky form factor and low usage coefficient. Even the smallest mobile phones are still hardly comfortable to carry in a pocket. Multifunctional devices (e.g. combined phone and PDA) are even larger and carrying several different devices even more uncomfortable. At the same time the majority of appliances are used only a few times a day for a very brief period of time. Thus, the user has to put up with considerable inconvenience carrying around devices that are switched off doing nothing useful over 90% of the time.

Wearable Computing is a new paradigm that aims to solve this problems [16, 20, 27, 31]. It relies on three key concepts:

Integration Seamless integration of electronic devices with the user's everyday outfit. Such an integration shall result in a system, that neither hinder the users physical activity nor has any undesired effect on his appearance. This means that the user shall be able to have the device with him and operation under all and any circumstances.

Interaction Novel Human Computer Interaction (HCI) concepts that allow the user to access the system without interference with his ability to interact with the environment. This means that unlike conventional mobile devices, a wearable system should be useful for tasks when the user needs to focus his attention and physical activity on the real world (e.g maintenance, sports, discussions).

Situational awareness Providing the system with the ability to model and recognize user activity and environmental conditions. This is a prerequisite to the implementation of new HCI concepts and also to making wearable devices autonomously perform tasks, such as the search for, delivery and collection of relevant information.

Implementing a system that combines above features is an open problem that involves a number of conflicting requirements. These include low energy consumption, high computational performance (e.g. for the realization of the new HCI concepts), scalable connectivity (e.g. for the inclusion of different sensors distributed over different body locations), extendibility and an ergonomic form factor, making the system virtually invisible [3, 4, 25]. This paper shows how these criteria have been dealt with in the design of a general purpose computing module, intended to be the core component of a variety of wearable systems and applications.

1.2 QBIC design approach

The key to our design philosophy is the realization that the user's outfit is actually a complex, hierarchical system that combines different 'device' classes with a wide range of application domains and functionalities. For each device class the user has well defined ideas about their expected life cycle, price ranges and the way he needs to treat it. He configures the system according to the situation and his personal preferences both statically (when getting dressed in the morning) and dynamically during the day. In doing so he is bound by a set of hard constraints on the body location and hierarchy (shirt before jacket) of the clothing pieces as well as soft criteria on their compatibility with each other and with the social context.

As detailed in the following sections, the above consideration together with computer architecture and functionality driven requirements have lead to the Q-Belt-Integrated-Computer (QBIC), designed at our Lab[1]. This system integrates the electronics in the buckle of a fully functional belt with the belt itself acting as an extension bus and mechanical support for add ons.

The wearability perspective formed the starting point for our design process, as the system must account for all requirements of a classic belt. The following mechanical considerations were mainly influenced by the combined wearable and ergonomic ideas.

From a functional point of view the design goal was to develop a multifunctional wearable computer with the ability to operate in various applications. Therefore system functionality and flexibility were emphasized during the complete process. The final computer design adheres to the technical constraints, e.g. limits in electronic miniaturization for the buckle design and system heat dissipation (see figure 1).

The wearability and ergonomic design phase has been concentrated around human design issues and requirements [7] and can be summarized as follows:

[1]Wearable Computing Lab., ETH Zurich, Switzerland, www.wearable.ethz.ch

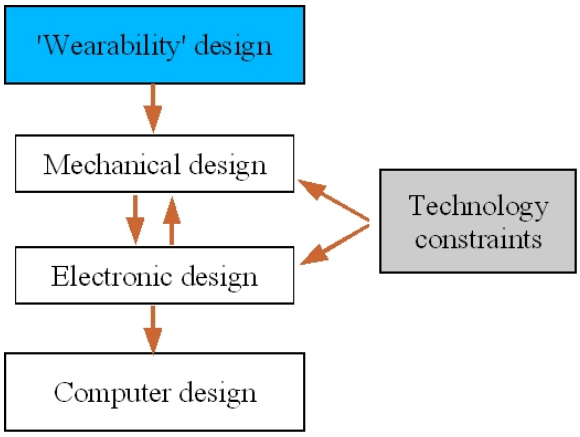

Figure 1. 'Wearability' driven design process

Comfort The system should under no circumstance hinder the user's physical activity. It may also not be perceived as aesthetically disturbing.

Flexibility It must be taken into account that the same computer might be used with different clothing configuration and aimed at different application domains.

Reliability As part of the user's outfit the system must be able to withstand a variety of environmental conditions and mechanical stress without becoming unreliable.

This process is further detailed in chapter 2. With regard to functionality and flexibility the following design properties were analyzed and incorporated into the system design:

Processing The system shall provide scalable computational performance to support applications with varying performance requirements. The applications require general purpose and signal processing functionality. For a wearable system it is important to evaluate processing performance in relation to energy consumption and heat dissipation.

Connectivity The system must support flexible communication interfaces to allow adaptation to application-specific I/O requirements. For various applications interfacing to a scalable number of sensors attached to the human body via wired interfaces (e.g. serial connection) or via wireless link (e.g. Bluetooth) must be possible. Additionally the interface bandwidth must be adaptable to support personal area network topologies with distributed local sensor subnets. These subnets may have different communication bandwidth needs when attached to a central wearable computer than direct interfacing to the sensors.

Extendibility Beside pure I/O connectivity the general extendibility with additional peripheral devices to add new capabilities must be solved in both the ergonomic and the functional domain regarding interface and connector types as well as device positioning (e.g. batteries).

Memory Sufficient memory (normally volatile RAM) for application-specific processing must be available. This memory might be extensible depending on the application. Typically the small form factor of a wearable computer may require direct soldering of RAM chips, prohibiting the extension option. Memory for storing sensor readings, user profiles or processing results shall be non-volatile, widely scalable in size and easy exchangeable by the user. Here typically FLASH-based memory is used.

1.3 Related work

Wearable systems and architectures are an active research area touching various other fields. According to the layer model for wearable system architectures, proposed by our group [15] this paper focuses on the mobile computing part (denoted as layer 2). Textile sensors (layer 1), embedded microsystems (layer 2) and peripheral devices (layer 3) will not be discussed.

Several approaches have been made in developing systems that address the specific wearable computing requirements. To date, no sufficient solution is available that satisfies all demands. Furthermore, in the relatively new field of wearable computing a general applicable wearable computer classification is missing.

Multiple intrinsic properties can be used to categorize wearables, including architecture, computational performance, application-type, energy consumption, connectivity and extendibility as well as ergonomic design properties. This overview will rely on general system architecture aspects, including functionality, ergonomic aspects and connectivity for sensor/device attachment.

Wearable computers currently available include PC-based and PDA-based systems relying on industrial standard architecture concepts. To this group belong PC-104-based systems, Systems based on Laptop and Mini-PC computers, e.g. Xybernaut [33], CharmIT Pro [6], VIA Wearable PC [30] and several PDA-based wearable systems, e.g. MIThril [17].

Wearable Systems based on *custom design* include low end *special purpose* appliances such as smart watches, badges [18, 19, 26], garments [24], medical monitors [5, 14] and *multiple purpose* wearable computers, providing more functionality and flexibility. To this group of wearable computers belong the LART [23], SPOT [8], ITSY [9] as well as both WearARM [2, 13] and QBIC.

Systems relying on standard PC- or PDA-based solutions do not reach a high degree of wearability, whereas the low end custom designs are bound to their specific task. The custom multiple purpose wearable computers establish a compromise between high and low end in providing processing performance and wearable system design. Of the custom multiple purpose systems available, only few address the ergonomic aspects, while providing sufficient connectivity options and computational performance, necessary for wearable applications. Figure 2 provides an overview regarding the described system types.

2 Ergonomic and mechanical design

2.1 Comfort

Wearable computers should under no circumstances diminish our comfort. The actual comfort of wearable computers depends on a variety of factors. A selection of these factors have been suggested by F. Gemperle et al. [7].

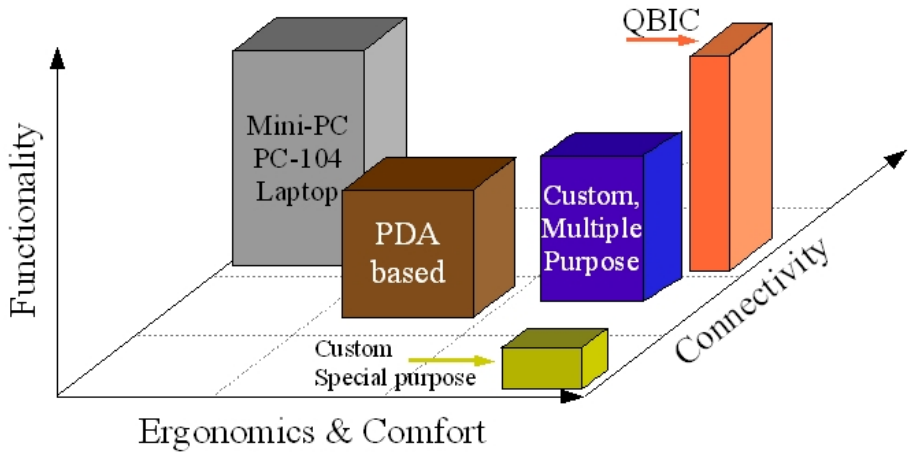

Figure 2. Classes of wearable computers

Clothing deals best with most of these factors, as it is available in all sizes, provides warmth, is often light, tends not to obstruct our movement, stays within the space we perceive as our body and is often aesthetically pleasing. In the realization of the wearable design idea it is important to select appropriate garment types (device classes) that satisfies our comfort perception.

A central position at the human body is of most worth regarding human body mass and acceleration as well as signaling distances for remote sensors. Positioning of devices at limbs will be perceived as obtrusive when device size and mass exceed low limits, e.g. wearing a watch at the wrist can be assumed as borderline for for size and weight at upper limbs and certain types of shoes may already be cumbersome for daily activities.

To maintain levels of comfort we decided to integrate our wearable computer into an ordinary accessory: a belt (see figure 3). As an accessory, a belt is not subject to typical cleaning procedures of normal clothes. Additionally it can be worn for both functional and aesthetic reasons.

As long as the above mentioned factors for the wearability of a belt remain the same, the best levels of comfort will be reached, using the guideline in table 1.

Element	Description
Placement	Within buckle or belt
Form Language	Should stay close to what we perceive as a belt
Human Movement	No change from an “ordinary” belt
Sizing	No change from an “ordinary” belt
Containment	No change from an “ordinary” belt
Attachment	Should fit within the loops of a pair of trousers
Weight	Waist is the right place to apply weight to the body, if necessary
Accessibility	A belt provides excellent accessibility
Sensory interaction	Most sensory interaction takes place elsewhere
Thermal	Heat dissipation/absorption needed
Aesthetics	Provide a variety of colors and materials
Long term use	Something that remains a question for later user tests

Table 1. Belt design evaluation list

Figure 3. The QBIC system in the buckle of a belt

This list clearly indicates what is of importance to our wearable computer: The functionality is *not limited to that of a computer* but it incorporates the uses of a belt, e.g. to support a pair of trousers and to embrace an aesthetic appearance.

Since various people prefer different styles we decided to create a variety of belts (different color, texture or material) with a similar buckle that incorporates the main electronic components (CPU, memory, wired and wireless interface drivers). The buckle can be taken off so the user can transfer the computer onto different belt types. When the user decides not to wear a belt at all (e.g. whilst wearing an evening dress or shorts) he/she can use the computer stand-alone, see drawing 4

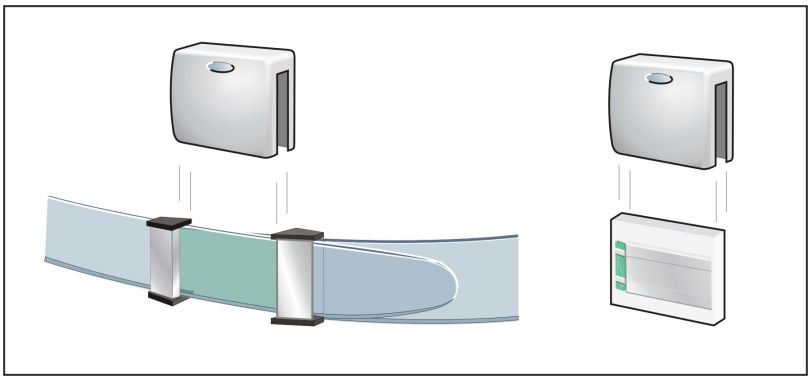

Figure 4. Left: the computer (buckle) is detachable from the belt and can be used stand-alone (right)

2.2 Flexibility

Wearable Computers should be able to assist us in a variety of activities of everyday life that can vary from shopping, sports and leisure to any professional related activities. Since each activity requires its own peripherals and computational power we decided to equip the QBIC with an exchangeable extension board and different belt types. Each belt may contain whichever peripherals are needed such as USB connectors, a serial connector or a VGA connector and a flat Li-polymer battery pack, see drawing 5.

If, for example, a certain task only requires a Bluetooth operated wrist mounted text display, the belt may just contain a battery. One could also decide to add more storage

space, an extra Bluetooth module or a PS/2 connection for a touch pad. To accommodate these extra functions the QBIC contains two circuit boards, a main board and an extension board. Both boards are connected to the belt via a standard 2mm PCB mounted connector, see drawing 6.

2.3 Reliability

People would not be able to rely on a tool that fails frequently, this means that a wearable computer should be electronically, mechanically and towards its software fail proof. The QBIC is constructed in such a way that the possibilities of mechanical failure are kept to a minimum. The clam-shaped buckle consists of three parts, a cover, a middle section and a back-side. The cover and the back are designed to be made out of a strong scratch-resistant plastic like polycarbonate or an acrylic plastic such as Acrylonitrile-Butadiene-Styrene (ABS) with a scratch-resistant coating. They are connected to each other with two long M3 screws. The middle section is made out of a 0.5mm stainless steel sheet, designed to dissipate the heat produced by the CPU. It fits tight into the outer parts to prevent dust or liquid to reach the PCBs, see figure 7.

The rather strong forces, a belt is subject to, are supported by the belt side of the buckle. The belt side consists of a strong (1mm thick) stainless steel section that houses the connector and a circuit board which leads the connections to the belt. The connector and the circuit board are fixed by two plastic parts that cover the stainless steel middle section. Extra space is left so the belt can be fed through the buckle.

2.4 Belt architecture

The belt of the QBIC consists of two layers of leather with a data cable in between. The data cable contains all possible power and data lines, whether used or not. The connectors are assembled according to the users specification onto a connector-block, which is pressed onto the data line in three possible locations. To provide good contact during use, the connector block is screwed onto a metal plate, which protects and compresses the delicate connection to the data cable.

In this way the belt is a part of the wearable computer, providing the extension bus in the philosophy of classical computer architecture. Beside this, the belt fulfills also the mechanical carrier function for external peripheral devices attached to the system and of course the traditional functionality of supporting a pair of trousers.

Our first version of the QBIC contains two connector blocks which incorporate a battery, a USB connector and some extra buttons and one connector block which only contains a VGA connector.

3 System architecture

3.1 Evaluation of the system architecture

In the system design phase emphasis has been drawn to the properties system performance, connectivity and extendibility. System performance features include the selection of an adequate processing unit, dimensioning of memory and interface speeds. Given the system size constraints, a System-on-Chip (SoC) main processor has been deemed most

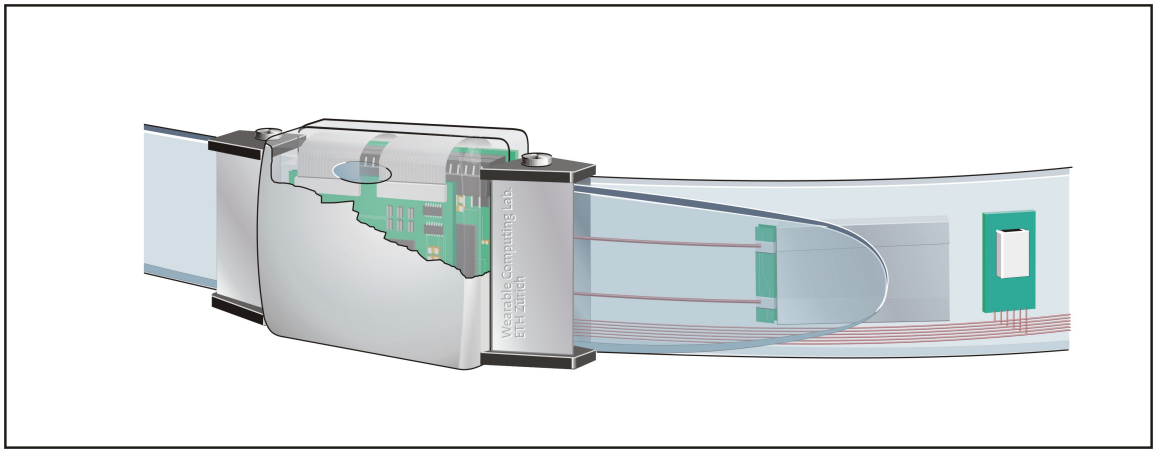

Figure 5. QBIC belt architecture

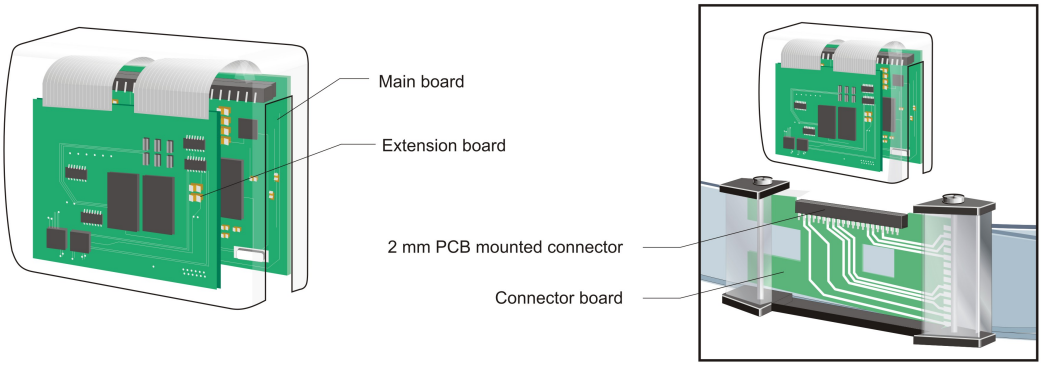

Figure 6. Buckle architecture

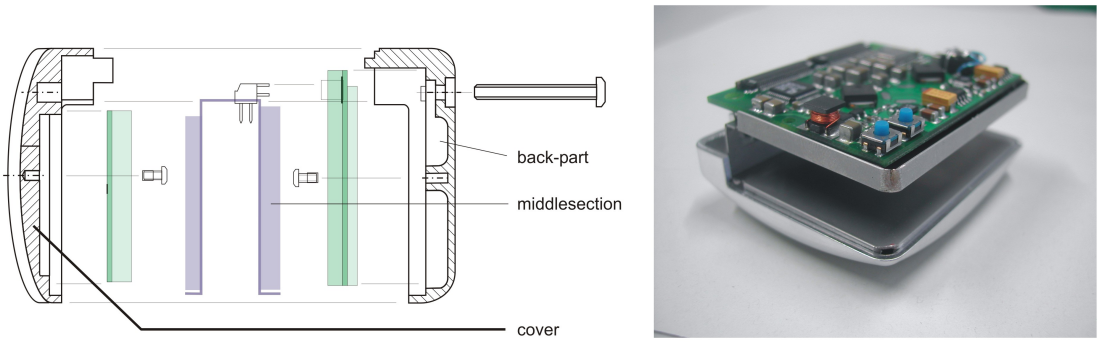

Figure 7. Mechanical structure of the buckle

appropriate to fulfill the requirements. Regarding the diversification of possible algorithms a general-purpose processor with an energy-efficient architecture and instruction set was valued higher than a Digital Signal Processor (DSP) architecture with several computational units running in parallel. A Field Programmable Gate Array (FPGA) could pose a valuable reconfigurable logic companion to off-load computational complex algorithms [22], with respect to the miniaturized system approach the device must have been omitted.

Connectivity and extendibility requirements have been addressed by equipping the system with wired and wireless interfaces. Scalability concerns to provide flexible sensor links have been included in the evaluation process as far as possible. As a result Serial interfaces based on commonly used EIA/TIA RS-232 have been integrated for wired sensor attachment. This interface type allows simple point-to-point operation, but requires converters to operate in a point-to-multipoint setup. The Universal Serial Bus (USB) has been selected as the default extension interface of the system, because it is a well-supported standard. In future more sensors may directly attach to the USB.

For the envisioned wearable system approach sensors or sensor networks will be integrated into garments. From a wearability perspective it will be easier to connect the different garments wirelessly. Therefore more emphasis has been paid to provide scalable wireless interfaces. A summary of all available user interfaces can be found in table 2.

A diagram of the QBIC system architecture is shown in figure 8. The following sections summarize the detailed system architecture and interface options.

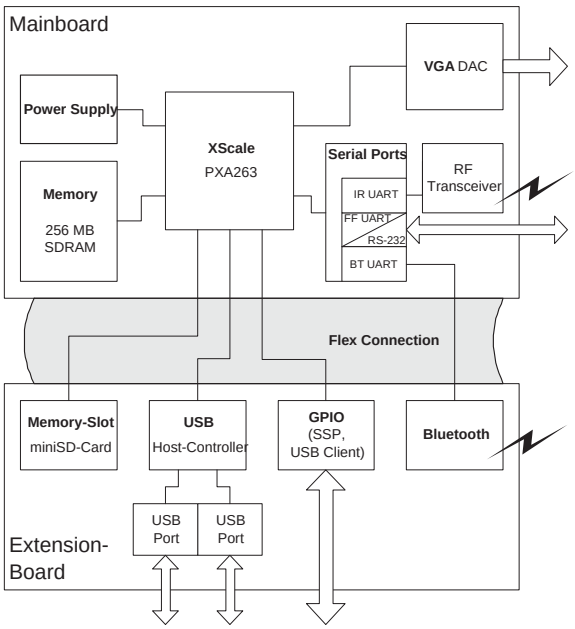

Figure 8. The QBIC system architecture

3.2 Mainboard design

The core of the system is an Intel XScale family processor: the PXA263B1C400. The power efficiency and experience with the previous wearable system WearARM [2,13], based on a Strong-ARM SA-1110 CPU, led to the selection of an ARM-core based XScale CPU.

Port	Function	Max. speed	Typ. power required [mW]
Serial Port	wired sensors interface	460 kbit/s	1.5
Bluetooth	wireless sensor interface	921.3 kbit/s	160 (active)
RF transceiver	wireless low-power sensor interface	19.2 / 115.2 kbit/s	26 (active)
USB Host	wired multi-function interface	12 Mbit/s	110 (excl. devices)
USB Client	wired base station interface	12 Mbit/s	integrated in CPU

Table 2. QBIC data interface summary

Main features of this processor include scalable clock frequency up to 400 MHz, dynamic core-voltage scheduling as well as several power-save modes. The PXA26x family utilizes the ARM v5TE architecture, which provides a set of integrated DSP instructions. These technologies are best suited for wearable computers, where a low energy consumption for a long battery lifetime is as important as the need of a high but also adaptable computing performance. A step-down converter is used to regulate CPU core voltage. Additionally the PXA263 offers 32 MBytes of internal FLASH memory for non-volatile storage of operating system, applications and user data.

There are four SDRAM ICs soldered onto the board providing a total capacity of 256 MBytes. Each partition is integrated into a single 512 Mbit chip (16M x 32Bit). This relatively large capacity for a mobile devices allows a wide range of future applications, also in the field of multimedia (audio and video processing). As the form factor of the system is very limited, providing a SDRAM extension option through additional connectors was not feasible. Instead, it was chosen to directly integrating a larger memory for compensation. This approach has the drawback of a higher power consumption for applications with low memory requirements.

The Intel PXA260-family has 3 integrated serial interfaces (UARTs): a full-functional, a Bluetooth and a infrared-UART. The full-functional UART is level-shifted on the mainboard and can be used as fully EIA/TIA RS-232 compatible serial port with up to 460 kbps. This 'old-fashioned' interface allows to attach standard periphery devices like a mouse or a modem, can be used as a I/O-console for the operating system shell or to connect wired sensor networks. The Bluetooth-UART is directly connected to the Bluetooth-Module on the extension board and handles up 921.3 kbps. The third UART is connected to a low power RF transceiver (TR1001 from RFM). This device works in the ISM-Band at 868 MHz and supports Amplitude Shift Keying (ASK) and On/Off-Keying (OOK). This kind of wireless communication consumes much less power than wireless LAN (WLAN) or even Bluetooth. Even though it reaches date rates between 19.2 kbps (OOK) and 115.2 kbps (ASK), which is sufficient for input devices with a relatively low data rate, like PS/2. Furthermore it is best suited as a master node for different kinds of sensor-networks distributed over the users body, e.g. PAD'Net [10].

Another important periphery interface on the mainboard is the VGA DAC. It converts the 16 digital signal lines from the PXA263 built-in LCD controller to an analog standard VGA-signal with a resolution of 640 x 480 pixels and 16bit color depth. VGA is still the standard display interface, which is not only used by common monitors (CRT) and LCDs but also for Head Mounted Displays (HMD), which are worn in front of the users eye(s) to provide a direct visualization interface.

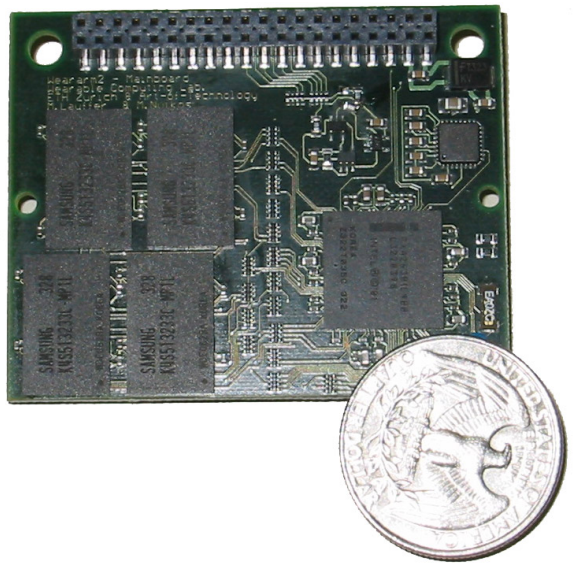

Figure 9. The QBIC main board

3.3 Extension board design

The extension board contains peripheral components that are essential for a majority of intended applications. As the extension board forms an optional part, different interfaces could be selected for certain applications. In principle, a different extension board could be implemented for every application domain.

In the default version of the board is a slot for a MiniSD storage card included to extend the built-in FLASH-Memory of the XScale processor. This type of FLASH Memory Cards is one of the smallest currently available on the market. It allows to integrate up to 256 MBytes on a size of 20x21.5 millimeters and a thickness of 1.4 millimeters. This memory is predestined to store user and sensor data or additional application software.

One of the most important functions on the default extension board is the USB host controller. Because there are innumerable USB devices on the market, it is the intended main peripheral interface. It can be used to attach external mass storage devices (USB memory sticks) which will provide additional space for bulk data, for a WLAN stick or either for any input/output device, including multimedia components. The USB host controller provides two independent ports and can handle USB low-speed and full-speed devices (1.5 and 12 Mbit/s). The USB host controller is connected to the CPU through a 16-Bit data bus.

For diversified wireless connections a Bluetooth module was integrated on the default extension board. This allows a wide range of possible applications as wireless Internet (through a Bluetooth Access Point or mobile phone), wireless display or any other Bluetooth input/output device. The used module is a class 2 device (transmit power typical 1.5 dBm for a range up to 10 meters) and is packaged in a small form-factor (10.5 x 15.5 millimeters). The main function of the Bluetooth port is linking sensors, sensor networks or a remote base station computer for management or data downloading from the wearable computer.

Additional general purpose IO (GPIO) pins from the processor are provided for future use, e.g. for a USB client function or communication with peripheral devices through the

Synchronous Serial Protocol (SSP).

A flexible substrate connects the extension board to the main board and is directly integrated into the substrate of the extension board which provides a high reliability connection.

3.4 Mechanical properties

In order to save power all interface chips can be switched off or set to idle mode by software while they are not used. Since wearable devices are expected to be integrated unobtrusive in everyday clothing they should be very small. Therefore all components were selected in their smallest available form factor, using ball grid packages where possible. As a result of a dense placement we achieved a PCB for the main board which is 44 by 55 millimeters in dimension. The extension board is even smaller and measures 48 x 31 millimeters (not including the flex connection).

To extract the system interfaces during software development a port replicator board was created which takes all connections from a single plug on the QBIC mainboard and distributes the interfaces to the designated connectors (2 USB, VGA, Serial, JTAG, Power). Additionally the board offers switches and two BCD displays connected to GPIO pins providing simple I/O facilities.

4 System software

4.1 Blob bootloader

To initialize the QBIC and to load an operating system kernel, the Boot Loader Object (BLOB) bootloader is used. BLOB has been originally developed by the LART group at the Technical University of Delft [23]. Its main advantage is a relatively easy extendibility and adaptability to a new platform. Basically, the BLOB initializes the QBIC hardware, loads Linux kernel and ramdisk and eventually starts the kernel. BLOB offers a command line feature controlled through the QBIC serial ports. Over this interface a new kernel, ramdisk or blob image can be downloaded and stored on the internal FLASH memory. The QBIC entire software is stored in the 32MB internal FLASH, since external mass storage or the MiniSD card are no mandatory part of the system. A memory map is shown in figure 10.

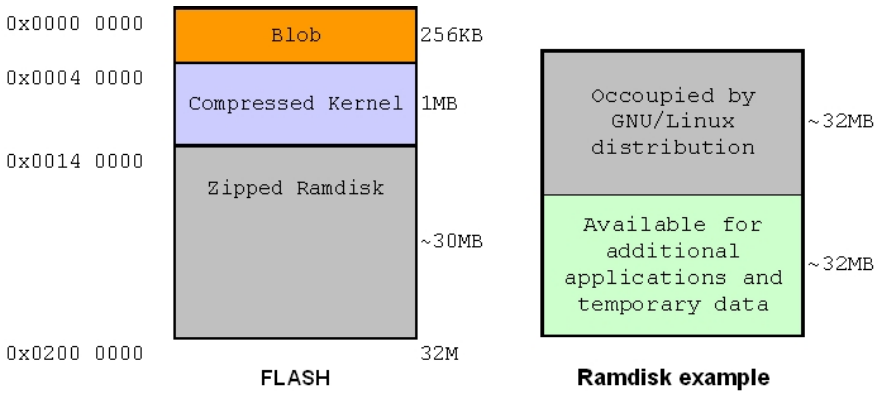

Figure 10. Memory layout of the QBIC FLASH and Ramdisk

4.2 GNU/Linux

The GNU/Linux system has been chosen as operating system (OS) foundation for the QBIC. Several reasons have led to this decision, most importantly because GNU tools and Linux are open source software with a wealth of information at disposal. The ARM architecture is greatly supported by Linux [11,32], as well as the large number of supported peripheral devices and interfaces.

The running system can be controlled through a serial console or through a Point-to Point Protocol (PPP) interface linked to one of the serial lines, enabling the QBIC to have a network connection with a host system for, e.g. telnet and secure shell, Network File System (NFS) mounting or Internet.

An LCD interface, that attaches to the DAC for VGA output, is driven by a frame buffer interface. Simple Graphical User Interfaces (GUI) can be build utilizing several available frame buffer libraries [12, 29].

4.3 File system

The root file system is a 64MByte EXT2-type ramdisk, that contains a Linux distribution with standard tools and applications. Of the ramdisk ∼32MByte remain available for additional applications and temporary data (see figure 10). In this setup 192MByte will remain as system memory. It is possible to devolve a larger amount of the system memory (256MByte) for the file system, to have more space for temporary files, e.g. data from sensors, intermediate calculations. For applications requiring more storage space, the MiniSD card (up to 256MB) or an mass media attached to the USB, e.g. USB memory stick can be used instantly, providing a storage capacity of several gigabytes.

Since a full sized PC distribution is not feasible for an embedded device, a minimal yet usable Linux distribution has been compiled. The ramdisk is loaded and expanded from a compressed file system stored in internal FLASH memory. The compressed file system inflates roughly with a ratio of 1:2. The size in the FLASH has been fixed to the maximum possible (∼30MByte), beside bootloader and kernel image (see figure 10).

The provision for a PPP link allows a NFS partition to be mounted on the QBIC (via serial cable or wirelessly using Bluetooth), thus overcoming the lack of space on the main file system in semi-static applications, where the host system is in near proximity.

Currently a Debian distribution is being ported to the QBIC, so that a common tool set and package manager ease the management of software on the system. This will also allow running a standard X Window installation, with different window managers or X Window-less windows manager like Qtopia on QBIC.

5 Implementation results

5.1 Power consumption

Power consumption is a well-known design issue in mobile systems. As stated before, a compromise between performance and energy requirements must be reached during system design. First measurement results were gained from a fully running mainboard.

Estimation of the most critical components indicate a total power budget of about 1.5W for the mainboard for operation at normal level (ambient temperature $T_{Amb} = 25\,^{\circ}\mathrm{C}$). For

the extension board, a consumption of about 270mW is required to operate Bluetooth and the USB host controller. Additional devices, optionally attached to the USB may require more power.

For power measurements the CPU was operating constantly at the maximum speed and frequency. Voltage scaling was not used so far. First measurements were made with the mainboard in different operating conditions shown in table 3. The results indicate, that different algorithms influence the power consumption, but the estimated 1.5W will not be overshot.

As the power consumption drops almost linear with the CPU frequency, the overall consumption can be analyzed in different duty cycles. This analysis must be supported with the integration of power management functions into the OS kernel.

Software	Power required [W]
Blob running	0.9
Linux Shell running	1.1
Linux kernel starting (peak)	1.4
Memory test	1.5

Table 3. Mainboard power measurements, $T_{Amb} = 25\,^{\circ}\mathrm{C}$

5.2 Heat dissipation

With the miniaturization of the system, integrating large amount of dynamic memory, a CPU with fast clock cycles, several interfaces and power supply in a small box the dissipation of heat becomes an increasing problem. This is especially valid, if the system is running under heavy load. From this point of view the operation conditions with extreme stress are of most interest. To measure the heat generation the processor was operated at maximum clock frequency of 400 MHz, SDRAM operated at 100 MHz.

The CPU is the hottest part in the system. Table 4 shows the measurement results of different chassis materials that were used to evaluate dissipation. Operated without chassis a CPU package temperature of about 57°C is reached ($T_{Amb} = 25\,^{\circ}\mathrm{C}$). This is about the same level as measured for a plastic chassis without metal plate for heat absorption (61°C) and virtually no air flow. A metal chassis, developed during early package evaluation yields a slightly lower package temperature, due to the better absorption capabilities of the housing.

Configuration	CPU package temperature
without chassis	$T_{CPU} = 57\,^{\circ}\mathrm{C}$
plastic chassis	$T_{CPU} = 61\,^{\circ}\mathrm{C}$
metal chassis	$T_{CPU} = 55\,^{\circ}\mathrm{C}$

Table 4. QBIC temperature measurements

Both plastic and metal housing are comfortable to wear permanently, without disturbance by heat, even at elevated load level. No significant influence on the power consump-

tion was detected during the tests with different housings.

6 Outlook

The QBIC belt integrated wearable computer exhibits excellent features as a research and test platform for wearable computing. More specifically, we will study situational awareness [1, 28] in various application domains. These fields include medical aiding systems, mobile worker assistance as well as security and rescue applications. Situational awareness requires gathering and storing sensor data and computing classification information based on pattern and statistical modeling (Context recognition). The QBIC computer is well designed to fit into these applications. Furthermore the requirements and functionality of wearable operating systems and power-aware computing will be studied.

A specific example, currently deploying the QBIC system, is the European IST FP6 MyHeart project [21]. Context awareness is used here to detect certain sport activity patterns, e.g. intensity, load and quality of exercise execution to prevent healthy people from entering the 'risk zone' for cardio-vascular diseases. Since permanently worn, the system can further act as a stress manager, extending the idea of exercise monitoring towards improving private and professional lifestyle. Continuous analysis of daily activities and supporting the user through direct feedback, e.g. how to integrate physical activity into the daily schedule, are a reasonable application field for this platform.

7 Acknowledgments

The authors would like to thank Matthias Nyikos from Art-of-Technology AG., Zurich, Switzerland (www.art-of-technology.ch) for supporting design and implementation of the QBIC hardware.

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